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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,360	01/14/2004	Ulrich Baier	INF-127	2353

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EXAMINER	
LEE, GRANVILL D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,360	BAIER ET AL.	
	Examiner	Art Unit	
	Granvill D. Lee Jr	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-20* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. In this case, drawings 1b-1d and 1f-1h, which depict a single layered substrate, are not claimed and it is not sure how they fit into the picture of the claimed invention. Explanation is required, as no new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 12 is objected to because of the following informalities: The claim cites three components (SiO_2,poly and SiO_2) to a layered stack, while only claiming two layers. Appropriate explanation or correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Brady et al.

In view of claim 14, Brady et al. teaches a mask for forming a set of deep structures and a set of shallow structures in a substrate (Col. 2 lines 17-23). This design comprises, a first set of larger features for forming the deep structures, a second set of smaller features for forming the shallower structures, wherein the deeper structures and the shallower structures are formed using the mask in a single lithography patterning step (Col. 2 lines 33-40).

In viewing claim 15, a first set and a second set of features are arranged to produce a set of related and self-aligned structures in the substrate (Col. 2 lines 3-17) as taught by Brady et al.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8, 11-12 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brady et al. in view of Evans et al.

In view of these claims, Brady et al. discloses a process (clms. 1 and 18) using a mask (clm. 14) for introducing structures in to substrate, where the structures contain a set of deep structures and a set of shallow structures (Col. 2 lines 20-30), comprising depositing on the substrate (Fig. 4 #50), a layer stack comprising at least one layer (#56) containing silicon oxide material (Col. 6 lines 35-45). Brady et al. places a photosensitive layer on the top of the layer stack (#60) and then patterns the photosensitive layer in a lithographic process using a mask with a set of smaller and a set of larger features (Col. 2 lines 50-60), which are developed in the photosensitive layer (Col. 4 lines 30-40). Brady et al. forms beneath the photosensitive layer a set of smaller openings and a set of larger openings and the etching includes the first layer of the silicon oxide layer down through the substrate (Fig. 6 #72 and #74).

However, Brady et al. fails to use a two-layer stack of different materials on the substrate. Evans et al. in forming a shallow trench uses a stack of at least two layers which are both etched down through to the substrate. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the single layered substrate of Brady et al. with that of a double layered substrate of Evans et al. with the objective of forming other components (i.e gate oxide etc.) of a device, using the additional layers. Brady et al. found that sub-sequential layers help to form

the device structure (Col. 1 lines 40-50) of increasing complexity, which would broaden the type of devices that could be made (Col. 5 lines 3-7).

In regard to claim 2, Brady et al. uses a process where the final etched layer is the substrate itself (Fig. 6).

In view of claim 3, Brady et al. uses a set of larger openings form a set of deep structures and a smaller set of openings form the shallow structures. (Col. 2 lines 35-40).

In view of claim 4, Brady et al. selectively etch the substrate and the adjacent layer where both the smaller and larger openings are formed in the substrate (Fig. 9 #70 and #72).

In view of claim 5, Brady et al. selectively etching the substrate down to a depth using the shallow structure (Col. 9 lines 59-67).

In viewing claim 6, Brady et al. deposits a blanket photosensitive layer on the small and large openings (Col. 8 line 55-Col. 9 line 10), removed followed by an etching down to the desired depth (Col. 7 lines 15-60).

In view of claims 7-8, Brady et al. uses an etching process, which forms inclined sidewalls (Fig. 6) at a slope angle between to surfaces (Col. 1 lines 40-50).

In view of claim 11, Brady et al. processes the second layer using a selective etching process where the etching rate is dependent on the depth or width or orientation of the structure (Col. 11 lines 1-14 & col. 1 line 63-Col. 2 line7).

In view of claim 12, Evans et al. discloses a silicon oxide layer (#12) and a polysilicon layer (#16) used in making the stack of the device.

In view of claim 17, Brady et al. depicts a set of larger features having at least one dimension greater than one dimension of the smaller set of features (Col. 6 lines 13-30).

Claims 13, 16 & 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brady et al. in view of Evans et al. and in further view of Shoda.

In view of these claims (esp. clms. 13, 16 & 19), Brady et al. develops a process for introducing structures in to substrate, where the structures contain a set of deep structures and a set of shallow structures. Evans et al. shows a process where a two-layered stack is used in conjunction with shallow trench structures. Yet, neither inventor shows a first set of features used for contact holes or, a second set of features for interconnects.

Shoda discloses a technique (Col. 6 lines 23-30) where device processing includes a set of features designed for contact holes and a second set of features for interconnects (Abstr.). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the teachings of both Evans et al. and Brady et al. in order to achieve multi-level contact structures while minimizing the process steps to make them (Col. 1 line 57-Col. 2 line 5). Shoda thought that the approach of forming multi-level

while more complex and costly, could possibly be simplified though the masking technique where both contact holes and interconnects can be made in a reduced number of steps (Col. 1 line 57-Col. 2 line 5).

In view of claim 20, Shoda deposits a metallic material in the smaller and larger structures (Col. 6 lines 19-33) and removing any excess metal from these structures (Col. 1 lines 27-33).

Allowable Subject Matter

Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
The following is an examiner's statement of reasons for allowance of these claims subject to above conditions: The prior art of record (i.e.Brady et al.) does suggest or discloses smaller and larger features made on a substrate, but the prior art fails to describe or suggest *inter alia* the invention of finding a predetermined width of a shallow structure (clm. 9) or a deep structure as calculated based on the formulas as claimed.

Contact Information

Any inquiry concerning this communication or earlier communications for the examiner should be directed to Granvill Lee whose telephone number is (571) 272-1897. The examiner can be

normally reached on Monday thru Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are not successful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Granvill Lee
Art Unit 2891

Gl
4/19/05